CLAIMS

1. A method for modifying the original logic design of an application specific integrated circuit having integrated circuit connection circuitry and at least one semiconductor layer and at least one metal layer, comprising:

determining what general purpose logic blocks will be used for programmable circuits included in the integrated circuit but not connected to the integrated circuit connection circuitry;

determining a location for the programmable circuits;

preparing at least one completed application specific integrated circuit with all layers and a plurality of programmable circuits and at least one application specific integrated circuit without the at least one metal layer;

testing the at least one completed application specific integrated circuit and identifying required design modifications;

determining what additional logic is needed to make the required design modifications and which of the plurality of programmable circuits combined with what configuration signals are required to implement this logic;

preparing a new metal mask to connect selectively the required programmable circuits to the integrated circuit connection circuitry; and

providing a source for the configuration signals required for the selectively connected programmable circuits to cause them to implement the desired logic.

2. The method of claim 1 wherein the act of providing a source for the configuration signals comprises providing configuration bits stored in a configuration register.

3. The method of claim 1 wherein the plurality of programmable circuits has configuration inputs and the act of providing the configuration signals comprises providing configuration bits stored in a configuration register to the configuration inputs.

4. The method of claim 2 wherein the integrated circuit is adapted for use in a personal computer and the act of providing a source for the configuration signals comprises providing configuration bits from the BIOS when the personal computer is booted up.

5. The method of claim 1 wherein the act of determining a location for the programmable circuits comprises determining a predefined pattern for placing the programmable circuits at multiple locations on the die area occupied by the integrated circuit.

6. The method of claim 1 wherein act of determining a location for the programmable circuits comprises determining a predefined pattern for placing the programmable circuits at multiple locations on the die area occupied by the integrated circuit such that the programmable circuits are distributed substantially throughout the die area occupied by the integrated circuit.

7. The method of claim 1 wherein act of determining a location for the programmable circuits comprises determining a predefined pattern for placing the

programmable circuits at multiple locations on the die area occupied by the integrated circuit such that the programmable circuits are located in proximity to a portion of the integrated circuit most likely to be modified.

8. The method of claim 1 wherein the integrated circuit is a standard cell ASIC.

9. A method for modifying the logic of an application specific integrated circuit having integrated circuit connection circuitry connecting a plurality of standard cells comprising:

(a) locating at least one programmable circuit on a die before the metal one stage;

(b) if logic modifications are needed, then connecting the at least one programmable circuit to the integrated circuit connection circuitry such that the design modifications may be implemented; and

(c) configuring the at least one programmable circuit such that the design modifications may be implemented.

10. The method of claim 9 wherein the act of connecting the at least one programmable circuit comprises connecting the at least one programmable circuit during the metal mask stage.

11. The method of claim 9 further comprising locating at least one configuration register on the die before the metal one stage, wherein the at least one programmable circuit is configured by bits stored in the configuration register.

12. The method of claim 11 wherein the configuration bits are stored in the at least one configuration register during a boot-up process.

13. The method of claim 9 wherein the act of locating the at least one programmable circuit comprises locating the at least one programmable circuit in a pattern defined by the likely location of logic modifications.

14. A method for designing an application specific integrated circuit comprising:

(a) locating a plurality of circuits on a die, wherein the plurality of circuits comprise a logic design;

(c) locating at least one programmable circuit on the die;

(d) determining whether modifications to the logic design are desired;

(e) if modifications to the logic design are desired, connecting the at least one programmable circuit to the plurality of circuits during a metal mask stage such that the modifications to the logic design may be implemented; and

(f) providing configuration signals for programming the at least one programmable circuit such that the modifications to the logic design may be implemented.

15. The method of claim 14, wherein the act of connecting the at least one programmable circuit comprises interconnecting the plurality of circuits by integrated circuit connection circuitry and connecting the at least one programmable circuit to the integrated circuit connection circuitry.

16. The method of claim 14, further comprising locating at least one configuration register on the die.

17. The method of claim 16 further comprising storing the configuration signals in the at least one configuration register.

18. The method of claim 14, wherein the act of locating the at least one programmable circuit on the die comprises determining what general purpose logic blocks will comprise the at least one programmable circuit.

19. The method of claim 14, wherein the act of determining whether modifications to the logic design are desired comprises testing a die upon which the plurality of circuits have been interconnected by integrated circuit connection circuitry.